

REMARKS

After entry of this amendment, claims 1-21, 23-30, and 32-33 remain pending. In the present Office Action, claims 1-4, 15-20, 24-29, and 33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al., "A Hardware Logic Simulation System" ("Agrawal_1"). Claims 5-14, 21, 23, 30, and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Agrawal_1 in view of Agrawal, et al, "Architecture and Design of the MARS Hardware Accelerator" ("Agrawal_2"). Applicants respectfully traverse these rejections and request reconsideration.

Claims 1-20 and 24-29

Applicants respectfully submit that each of claims 1-20 and 24-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "each node of the plurality of nodes is configured to cause the simulator program to evaluate the model during the second phase in response to receiving a command during the second phase, the command including one or more signal values for signals of the model".

The Office Action alleges that the first phase of claim 1 is the fan-out update phase and the second phase of claim 1 is the evaluate phase, as described in Agrawal_1, section 2.1, page 20. Applicants respectfully disagree. Agrawal_1 teaches "During the fan-out phase, each event scheduled for the current time, t, is processed by updating the value of a specified signal and scheduling all gates in the fan-out list of this signal for evaluation...processing events in two phases permits all input changes at one gate to be accumulated before that gate is evaluated...each gate scheduled during the fan-out update phase is evaluated during the evaluation phase. If the evaluation results in a new value of the gate output that differs from the current value, an event is scheduled on the gate output signal. This event will be processed during some subsequent fan-out update phase." (Agrawal_1, section 2.1, second paragraph, page 20).

From the cited section, it is clear that all input signal values are processed during the fan-out update phase in Agrawal_1. Any output signals determined during the

evaluation phase are provided to a later fan-out update phase. Accordingly, no signal values are provided for a model during the evaluate phase. Therefore, Agrawal_1 does not teach or suggest "each node of the plurality of nodes is configured to cause the simulator program to evaluate the model during the second phase in response to receiving a command during the second phase, the command including one or more signal values for signals of the model" as recited in claim 1.

Additionally, the Office Action asserts that the plurality of nodes recited in claim 1 are anticipated by the PEs in Agrawal_1. Applicants respectfully submit that Agrawal_1's PEs do not teach or suggest "a plurality of nodes, wherein each node of the plurality of nodes is configured to simulate a different portion of a system under test using a simulator program". Rather, the PEs are operated in a pipeline fashion to perform different pipeline stages of a single simulation. For example, Agrawal_1 teaches that "Fig. 2 shows how the two-phase simulation algorithm is partitioned for implementation on the MARS hardware accelerator...Each block in the figure corresponds to a single PE that has been microcoded to perform the specified function" (Agrawal_1, section 2.2, third paragraph, page 20). Thus, Agrawal_1's PEs are each programmed to perform a portion of the fan-out update/evaluate algorithm, not a different portion of the system under test.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-14 depend from claim 1, and thus are patentable over Agrawal_1 for at least the above stated reasons as well. Each of claims 2-14 recites additional combinations of features not taught or suggested in the cited art.

Claim 15 recites a combination of features including: "cause the simulator program to evaluate the model during a second phase of the timestep in response to receiving a second command including one or more signal values for signals of the model, wherein the second command is received during the second phase of the timestep". The same teachings of Agrawal_1 highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 15. Applicants respectfully

submit that Agrawal_1 does not teach or suggest the above highlighted features of claim 15, either. Accordingly, claim 15 is patentable over the cited art. Claims 16-20, being dependent from claim 15, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 16-20 recites additional combinations of features not taught or suggested in the cited art.

Claim 24 recites a combination of features including: "receiving a second command during a second phase of the timestep; and processing the second command including causing the simulator program to evaluate the model if the second command includes one or more signal values for signals of the model." The same teachings of Agrawal_1 highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 24. Applicants respectfully submit that Agrawal_1 does not teach or suggest the above highlighted features of claim 24, either. Accordingly, claim 24 is patentable over the cited art. Claims 25-29, being dependent from claim 24, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 25-29 recites additional combinations of features not taught or suggested in the cited art.

Claims 21, 23, 30, and 32

Applicants respectfully submit that each of claims 21, 23, 30, and 32 recite combinations of features not taught or suggested in the cited art. For example, claim 21 recites a combination of features including: "signal the end of either the first phase or the second phase responsive to receiving a no-operation packet from each of the plurality of nodes subsequent to transmitting a command other than a no-operation packet to at least one of the plurality of nodes".

The Office Action alleges that Agrawal_1 teaches a no-operation packet as the "zero message" that is sent down the pipeline at the end of the evaluation to reconfigure the pipeline for the next fan-out update phase, citing section 2.2.2 of Agrawal_1. Agrawal teaches that the gate scheduler sends a zero message down the pipeline when the stack of gates that have been scheduled for evaluation is empty. (See Agrawal_1, section

2.2.2, page 21, left column, last two paragraphs). Thus, the end of the phase is detected by the emptying of a stack. This has nothing to do with signaling the end of a phase "responsive to receiving a no-operation command from each of the plurality of nodes", as recited in claim 21.

For at least the above stated reasons, Applicants submit that claim 21 is patentable over the cited art. Claim 23, being dependent from 21, is similarly patentable over the cited art for at least the above stated reasons as well. Claim 23 recites an additional combination of features not taught or suggested in the cited art.

Claim 30 recites a combination of features including: "signaling an end of a first phase of a timestep in a distributed simulation system by a hub of the distributed simulation system, ... wherein signaling the end of the first phase is responsive to receiving a no-operation packet from each of the plurality of nodes subsequent to transmitting a command other than a no-operation packet to at least one of the plurality of nodes". The same teachings of Agrawal_1 highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 30. Applicants respectfully submit that Agrawal_1 does not teach or suggest the above highlighted features of claim 30, either. Accordingly, claim 30 is patentable over the cited art. Claim 32, being dependent from claim 30, is similarly patentable over the cited art for at least the above stated reasons. Claim 32 recites an additional combination of features not taught or suggested in the cited art.

Claim 33

Claim 33 recites a combination of features including: "a first node of the plurality of nodes is configured to cause the simulator program to evaluate the model in response to receiving a first command including one or more signal values for signals of the model during a first timestep, and wherein the first node is configured to cause the simulator program to re-evaluate the model in response to receiving a second command including one or more signal values for signals of the model during the first timestep". The Office Action alleges that Agrawal_1 teaches the above highlighted features, citing the fan-out

update and evaluation phases of section 2.1 of Agrawal_1. Applicants respectfully disagree.

Agrawal_1 teaches "During the fan-out phase, each event scheduled for the current time, t , is processed by updating the value of a specified signal and scheduling all gates in the fan-out list of this signal for evaluation. Since several inputs of a gate may change simultaneously, a check must be made to avoid scheduling a gate more than once. Processing events in two phases permits all input changes at one gate to be accumulated before that gate is evaluated. This prevents multiple evaluations that might cause erroneous results. Each gate scheduled during the fan-out update phase is evaluated during the evaluation phase. If the evaluation results in a new value of the gate output that differs from the current value, an event is scheduled on the gate output signal. This event will be processed during some subsequent fan-out update phase. Once all scheduled gates are evaluated the simulator advances to the next time step and cancels any spurious events scheduled for this timestep." (Agrawal_1, section 2.1, second paragraph, page 20).

Thus, Agrawal_1 teaches a fan-out update phase in which all input signals are updated, followed by an evaluation phase in which the model is evaluated once. Explicit checks are made to prevent multiple evaluations of even a gate. If the evaluation causes a signal value to change, the change is scheduled for a subsequent time step. Once the evaluation completes, the simulator advances to the next time step. Nothing in this section teaches or suggests "a first node of the plurality of nodes is configured to cause the simulator program to evaluate the model in response to receiving a first command including one or more signal values for signals of the model during a first timestep, and wherein the first node is configured to cause the simulator program to re-evaluate the model in response to receiving a second command including one or more signal values for signals of the model during the first timestep".

Furthermore, as highlighted above with regard to claim 1, Agrawal_1 teaches that all signal values are received during the fan-out phase. Accordingly, a reevaluation due

to signal values received during the first timestep is not possible, since all signal values are received during the fan-out phase and a single evaluation is performed after all signal values are received. For at least all of the above stated reasons, Applicants submit that claim 33 is patentable over the cited art.

Information Disclosure Statement (IDS)

Applicants received the PTO-1449 form from the IDS filed October 20, 2005, with the present Office Action. However, the form is missing the Examiner's initials next to references D1-D4. Since the references are not crossed out, Applicants presume that this is merely an oversight. Applicants have included a copy of the PTO-1449 form herewith, with the missing initials highlighted. Applicants respectfully request that the Examiner initial the references to evidence their consideration.

Applicants note that an additional IDS was filed on July 21, 2005. Applicants respectfully request consideration of the IDS. Applicants have included a duplicate copy of the PTO-1449 form from the IDS, along with a copy of the date-stamped postcard evidencing receipt of the IDS on July 25, 2005. Applicants respectfully request consideration of the IDS and a return of the PTO-1449 form included therewith, initialed and signed by the Examiner to evidence such consideration.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-97900/LJM.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Request for Approval of Drawing Changes
- ☐ Notice of Change of Address
- ☐ Please debit the deposit account listed above in the amount of \$ for fees ().
- ☒ Other: Previously submitted PTO-1449 forms and copy of date-stamped postcard corresponding to one of the forms.

Respectfully submitted,



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